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10/675,027	09/30/2003	Dennis Kim	RAMB-01016US0	5412

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EXAMINER	
PANWALKAR, VINEETA S	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,027	KIM ET AL.	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-28* is/are allowed.

6)☒ Claim(s) *1-3,6-9,11,13-24 and 29-33* is/are rejected.

7)☒ Claim(s) *4,5,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 14 and 18 are objected to because of the following informalities:

1a. Regarding claim 14, it is suggested that in line 14 of the claim (line 21 on page 25) "outputting" be replaced by ---of outputting---.

1b. Regarding claim 18, it is suggested that in line 23 of the claim (line 2 on page 27)"an adjustable" be replaced by ---the adjustable---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 14-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2a. Regarding claim 14, it appears from Fig. 1 as if claimed first stage outputs signal in response to sampled data and not the data signal as claimed. (Line 8 of claim i.e. line 15 on page 26).

2b. Claims 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being dependent on claim 14.

2c. Regarding claim 18, it appears from Fig. 1 as if claimed first stage outputs signal in response to sampled data and not the data signal as claimed.

(Line 8 of claim i.e. line 16 on page 25).

2b. Claims 19-24 are rejected under 35 U.S.C. 112, second paragraph, as being dependent on claim 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 6-9, 13, 29-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Beherns (US 5572558).

3a. Regarding claim 1, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a clock circuit comprising:

- a clock circuit (Fig. 3, unit 28 is interpreted as the claimed clock circuit) capable of generating a clock signal in response to an adjustable phase step-size (VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase of

the clock signal and is hence interpreted as the claimed adjustable phase step-size); and

- a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate (The analog to digital converter (A/D) 24 is the claimed sampler. It receives the analog read signal 11. The data rate of the signal is varying.(Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data.)).

(See Fig.3 and column 8, lines 15-30).

3b. Regarding claim 2, Beherns further discloses the circuit wherein:

- the clock circuit includes a phase adjust step-size logic capable of outputting an adjustable magnitude of the phase step-size in response to the variable data bit-rate (Fig. 3, phase error detector F54, provides a phase error signal F123 indicating the amount (claimed step-size) of adjustment required to be made to the phase of the clock signal. It takes into account the variable data bit-rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal).

(See Fig.3 and column 8, lines 15-30).

3c. Regarding claim 3, Beherns further discloses the circuit wherein:

- the phase adjust step-size logic is capable of outputting an adjustable direction of the phase step-size in response to the variable data bit-rate The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase of the clock signal and is hence interpreted as the claimed adjustable phase step-size. Thus, it inherently indicates whether the phase should be increased or decreased. This interpreted as the claimed adjustable direction).

(See Fig.3 and column 8, lines 15-30).

3d. Regarding claim 6, no criticality is shown in choosing the claimed range of values (0 ppm –5000ppm). It appears as if the values have been chosen only as an example to demonstrate the variation in data rate. Hence the variation is data rate shown by Beherns reads on the claim (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data).

3e. Regarding claim 7, Beherns discloses the circuit, wherein:

- the adjustable phase step-size is adjusted in response to a first step-size corresponding to data phase drift and a second step-size corresponding to the variable data bit-rate (Fig. 3, phase error detector F54, provides a phase error signal F123 indicating the amount (claimed first step-size) of adjustment required to be made to the

phase of the clock signal. A phase error signal inherently indicates the amount by which the phase has drifted. Frequency error detector F52 provides a frequency error signal F124 indicating the amount (claimed second step-size) of adjustment required to be made to the frequency of the clock signal. It takes into account the variable data bit-rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal. Frequency error is inherently the amount by which the frequency or rate of the signal varies).

(See Fig.3 and column 8, lines 15-30).

3f. Regarding claim 8, Beherns also shows the circuit wherein:

- the first step size and the second step-size are summed to obtain the adjustable phase step-size (Fig. 3. PID loop filter F56 sums the two signals F123 and F124 to form signal 23, which adjusts the sampling clock. See Fig. 9B and column 9, line 21 – column 10, line 63).

(See Fig.3 and column 8, lines 15-30).

3g. Regarding claim 9, Beherns discloses the circuit wherein:

the clock circuit includes an indicator capable of adjusting the adjustable phase step-size responsive to the variable data bit-rate (Fig. 3, phase error detector F54, provides a phase error signal F123 indicating the amount (claimed step-size) of adjustment required to be made to the

phase of the clock signal and is hence interpreted as the claimed indicator. It takes into account the variable data bit-rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal).

(See Fig.3 and column 8, lines 15-30).

3h. Regarding claim 13, Beherns further discloses the circuit wherein:

- the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal (Broadly speaking, Fig.1 shows a system wherein data is encoded using units 4,6,10 and 14 to form symbols 16 that are transmitted via magnetic recording channel 18 and received in order to be decoded. Fig.3 also shows the circuit that receives encoded data and performs timing recovery in the receiver).

3i. Regarding claim 29, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed an apparatus comprising:

- a transmit circuit capable of transmitting a data signal having a variable rate (Broadly speaking, Fig.1 shows a system wherein data is encoded using units 4,6,10 and 14 (claimed transmit circuit) to form symbols 16 (claimed data signal) that are transmitted via magnetic recording channel 18. The data rate of the signal is varying. (Column 5, lines 1-

23 explain how the data rate varies from track to track of the disk which stores the data)).

- A receive circuit capable of generating a clock signal in response to the data signal.(Fig.3 also shows the circuit that receives data encoded by a system such as the transmitter of Fig.1 and performs timing recovery and is hence interpreted as the claimed receive circuit).
- wherein the receive circuit includes:
- a sampler, capable of receiving, in response to the clock signal, in response to the clock signal (The analog to digital converter (A/D) 24 is the claimed sampler. VFO F50 provides a clock signal to the sampling device 24. It receives the analog read signal 11.).
- a clock circuit, coupled to the sampler, (Fig. 3, unit 28 is interpreted as the claimed clock circuit) capable of generating a clock signal in response to an adjustable phase step-size (VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase of the clock signal and is hence interpreted as the claimed adjustable phase step-size).

(See Fig.3 and column 8, lines 15-30).

3j. Regarding claim 30, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a method for tracking a variable data rate signal (The data rate of the signal is varying. (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data)) comprising the steps of:

- receiving the signal .(Fig.3 shows the circuit that receives data 11 and performs timing recovery).;
- selecting an update rate(Fig. 3, unit 28 is clock circuit comprising VFO F50. VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. Thus, the timing recovery loop synchronizes values sampled by the sampling device 24 at a rate determined by the VFO F50. This is interpreted as the claimed selecting of an update rate); and
- selecting an adjustable step-size for an adjust signal responsive to the signal (Fig. 3, unit 28 is clock circuit comprising VFO F50. VF50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase and frequency of the clock signal

and this operation is hence interpreted as the claimed selecting of adjustable step-size for an adjust signal).

(See Fig.3 and column 8, lines 15-30).

3k. Regarding claim 31, Beherns further shows the method wherein the receiving step includes:

- sampling the signal in response to the adjust signal (The analog to digital converter (A/D) 24 performs the claimed sampling. It receives the analog read signal 11).

3l. Regarding claim 32, Beherns also shows the method wherein selecting an adjustable step-size includes:

- determining a first step-size based on the variable data bit- rate of the signal (Fig. 3, phase error detector F54, provides a phase error signal F123 indicating the amount (claimed first step-size) of adjustment required to be made to the phase of the clock signal. It takes into account the variable data bit-rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal);
- determining a second step-size (Fig. 3, frequency error detector F52 provides a frequency error signal F124 indicating the amount (claimed second step-size) of adjustment required to be made to the frequency of the clock signal);

- summing the first and second step-sizes to obtain the adjustable step-size (Fig. 3. PID loop filter F56 sums the two signals F123 and F124 to form signal 23, which adjusts the sampling clock. See Fig. 9B and column 9, line 21 – column 10, line 63).

(See Fig.3 and column 8, lines 15-30).

3m. Regarding claim 33, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a clock circuit (claimed device) comprising:

- a sampler capable of obtaining a signal having a variable data bit-rate in response to a clock signal (The analog to digital converter (A/D) 24 is the claimed sampler. VFO F50 provides a clock signal to the sampling device 24. It receives the analog read signal 11 with varying data rate (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data)); and
- means for adjusting the clock signal in response to the variable data bit-rate (Fig. 3, unit 28 is capable of generating a clock signal in response to an adjustable phase step-size. VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The error detectors take into account the variable data rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal).

(See Fig.3 and column 8, lines 15-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beherns.

4a. Regarding claim 11, Beherns discloses all the limitations claimed (See paragraph 3g above). Although Beherns does not explicitly disclose whether the indicator includes a state machine for detecting the variable data-bit rate, it is a well known fact that synchronizers and timing recovery circuits such as the one disclosed by Beherns can be implemented on state machines.[1]

Thus, it would have been obvious at the time the invention was made to use state machines in the clock circuit because the states in the state machine store information about the past and reflect the input changes from the system start to the present moment and aide in modelling of the application behaviour.

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[1] Few references showing state machines in clock circuits:
- Kozoil (US 3773975)
- Chen (US 5987238)
- Ramey (US 6104251)
- Brugel et al., "Variable Bandwidth DPLL Bit Synchronizer with Rapid Acquisition Implemented as a Finite State Machine" IEEE Transactions on Communications, vol. 42, No. 9, Sep. 1994, pp. 2751-2759

Allowable Subject Matter

5. Claims 4,5,10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

5a. Regarding claim 4, prior art of record fails to show a circuit comprising a clock generating circuit and sampler and including at least four stages wherein the clock circuit includes stall logic for capable of holding the third and fourth stage outputs in response to the first and second stage outputs, in combination with every other limitation of the claim and base claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

5b. Claim 5 will be allowable as being dependent on claim 4.

5c. Regarding claim 10, prior art of record fails to show the circuit wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step size and the second step size are summed to obtain the adjustable phase step-size, in combination with every other limitation of the claim and base claim. The claim is interpreted in light of the specification, especially Figs. 1 and 7.

5d. Regarding claim 12, prior art of record fails to show the circuit wherein the clock circuit includes an averaging circuit capable of averaging a plurality of up signals to obtain an average up value and a plurality of down signals to obtain an average down value, and outputting an adjust signal having the selectable phase adjust size in response to a comparison of the average up value and the average down value, in combination with every other limitation of the claim and base claim. The claim is interpreted in light of the specification, especially Figs 1 and 10 and page 19, line 15 – page 20, line 18.

6. Claims 14-24 will be allowed if the claim objections and 35 U.S.C. 112, second paragraph rejections in sections 1 and 2 of this office action are overcome. The following is a statement of reasons for the indication of allowable subject matter:

6a. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable a second stage output signal in response to the first of outputting stage output signal', a third stage, coupled to the second stage, capable outputting the phase adjust signal in response to the second stage output signal; and stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output

signals, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

6b. Claims 15-17 will be allowable as being dependent on claim 14.

6c. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal; a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal; stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals; an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit- rate; and, a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having an adjustable step-size responsive to the first and second step-sizes, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1, 5 and 7.

6d. Claims 18-24 will be allowable as being dependent on claim 18.

7. Claims 25-28 are allowed.

The following is an examiner's statement of reasons for allowance:

7a. Regarding claim 25, prior art of record fails to show a circuit with a clock circuit comprising an averaging circuit capable to output the phase adjust signal in response to an average up signal, obtained from up signals in a predetermined period of time, and an average down signal, obtained from down signal in the predetermined period of time, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 10 and page 19, line 15 – page 20, line 18.

7b. Claims 26 and 27 are allowable as being dependent on claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Chen (US 6041090) shows a data sampling and recover device in a PLL with a clock generator.

- Schmatz et al. (US 2003/0128786 A1) disclose a clock data recovery system for resampling a clock signal according to an incoming data signal stream.
- Tanji et al. (US 6307906 B1) show a clock and data recovery scheme for multi-channel, multi-rate communication receivers.
- Su et al. (US 6366628 B1) disclose a method and circuit for sampling timing recovery using phase and frequency errors.
- Boerstler et al. (US 6963629 B2) show an adaptive PLL with up and down signals charging the charge pump.
- Casper et al. (US 5838749) show a method and apparatus for extracting embedded clock from a digital data signal using state machine logic and having data with variable data rate.
- Beherns et al. (US 5754352) show a timing recovery PLL employing state machine logic.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-

3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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